

**DATA PROCESSING SYSTEM WITH REGISTER  
STORE/LOAD UTILIZING DATA PACKING/UNPACKING**

**ABSTRACT OF THE DISCLOSURE**

1       A data processing system (e.g., microprocessor **30**) for  
2       packing register data while storing it to memory and  
3       unpacking data read from memory while loading it into  
4       registers using single processor instructions. The system  
5       comprises a memory (**42**) and a central processing unit core  
6       (**44**) with at least one register file (**76**). The core is  
7       responsive to a load instruction (e.g., LDW\_BH[U]  
8       instruction **184**) to retrieve at least one data word from  
9       memory and parse the data word over selected parts of at  
10      least two data registers in the register file. The core is  
11      responsive to a store instruction (e.g., STBH\_W instruction  
12      **198**) to concatenate data from selected parts of at least two  
13      data registers into at least one data word and save the data  
14      word to memory. The number of data registers is greater  
15      than the number of data words parsed into or concatenated  
16      from the data registers. Both memory storage space and  
17      central processor unit resources are utilized efficiently  
18      when working with packed data. A single store or load  
19      instruction can perform all of the tasks that used to take  
20      several instructions, while at the same time conserving  
21      memory space.